

TM2G0080120K

1200V N-Channel Silicon Carbide Power MOSFET

V_{DS}	=	1200 V
$R_{DS(on)}$	=	80 mΩ
I_D	=	42 A

Features

- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Easy to parallel
- RoHS compliant

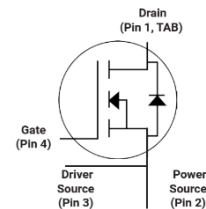
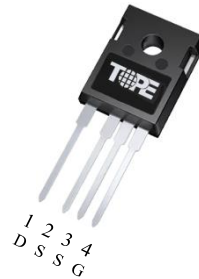
Benefits

- Higher System Efficiency
- Reduce cooling requirements
- Increased power density
- Enabling higher frequency
- Minimize gate ringing
- Reduction of system complexity and cost

Applications

- Switch Mode Power Supplies
- DC/DC converters
- Solar Inverters
- Battery Chargers
- Motor Drives

Package



Part Number	Package	Marking
TM2G0080120K	TO-247-4	TM2G0080120K

Maximum Ratings ($T_c = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain-Source Breakdown Voltage	1200	V	$V_{GS}=0\text{ V}$, $I_D=100\text{ }\mu\text{A}$	
I_D	Continuous Drain Current	42	A	$V_{GS}=20\text{ V}$, $T_c=25\text{ }^\circ\text{C}$	Fig. 18
P_D	Power Dissipation	208	W	$T_c=25\text{ }^\circ\text{C}$	Fig. 19
$V_{GS,op}$	Recommend Gate Source Voltage	-5/+20	V		
V_{GSmax}	Maximum Gate Source Voltage	-10/+25	V	AC ($f>1\text{Hz}$)	Note 1
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to +175	$^\circ\text{C}$		
T_L	Soldering Temperature	260	$^\circ\text{C}$		

Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
Static							
BV_{DS}	Drain-Source Breakdown Voltage	1200	--	--	V	$V_{GS}=0\text{ V}, I_D=100\ \mu\text{A}$	
I_{DSS}	Zero Gate Voltage Drain Current	--	11	100	μA	$V_{DS}=1200\text{ V}, V_{GS}=0\text{ V}$	
I_{GSS}	Gate-Source Leakage	--	10	250	nA	$V_{GS}=20\text{ V}$	
$V_{GS(th)}$	Gate-Source Threshold Voltage	2	--	4	V	$I_D=5\text{ mA}, V_{GS}=V_{DS}$	Fig. 11
$R_{DS(on)}$	Drain-Source On-Resistance	--	78	100	m Ω	$V_{GS}=20\text{ V}, I_D=20\text{ A}$	Fig. 6
Dynamic							
C_{iss}	Input Capacitance	--	1128	--	pF	$V_{GS}=0\text{ V}, V_{DS}=1000\text{ V}$ $f=1.0\text{ MHz}, V_{AC}=25\text{ mV}$	Fig. 17
C_{oss}	Output Capacitance	--	86	--			
C_{rss}	Reverse Transfer Capacitance	--	5	--			
E_{OSS}	C_{OSS} Stored Energy	--	44	--	μJ		Fig. 16
Q_g	Total Gate Charge	--	52	--	nC	$V_{DS}=800\text{ V}$ $I_D=20\text{ A}$ $V_{GS}=-5/+20\text{ V}$	Fig. 12
Q_{gs}	Gate-Source Charge	--	17	--			
Q_{gd}	Gate-Drain Charge	--	15	--			
$t_{d(on)}$	Turn-on Delay Time	--	35	--	ns	$V_{DS}=800\text{ V}$ $V_{GS}=-5/+20\text{ V}$ $I_D=20\text{ A}$ $R_{G(ext)}=2.5\ \Omega$	
t_r	Turn-on Rise Time	--	16	--			
$t_{d(off)}$	Turn-off Delay Time	--	43	--			
t_f	Turn-off Fall Time	--	12	--			
$R_{G(int)}$	Internal Gate Resistance	--	4.0	--	Ω	$f=1.0\text{ MHz}, V_{AC}=25\text{ mV}$	

Body Diode Characteristics ,at $T_J=25^\circ\text{C}$, unless otherwise noted

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
I_S	Continuous Diode Forward Current	--	--	42	A		Note 1
V_{SD}	Diode Forward Voltage	--	4.0	--	V	$V_{GS}=0\text{ V}, I_S=10\text{ A}$	Fig. 8, 9, 10
t_{rr}	Reverse Recovery Time	--	26	--	ns	$I_S=20\text{ A}, V_{DS}=800\text{ V}$ $V_{GS}=-5\text{ V}$ $di/dt=2100\text{ A/us}$	Note 1
Q_{rr}	Reverse Recovery Charge	--	163	--	nC		
I_{rrm}	Peak Reverse Recovery Current	--	12	--	A		

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	/	0.68	/	$^\circ\text{C/W}$	Fig. 20

Typical Performance

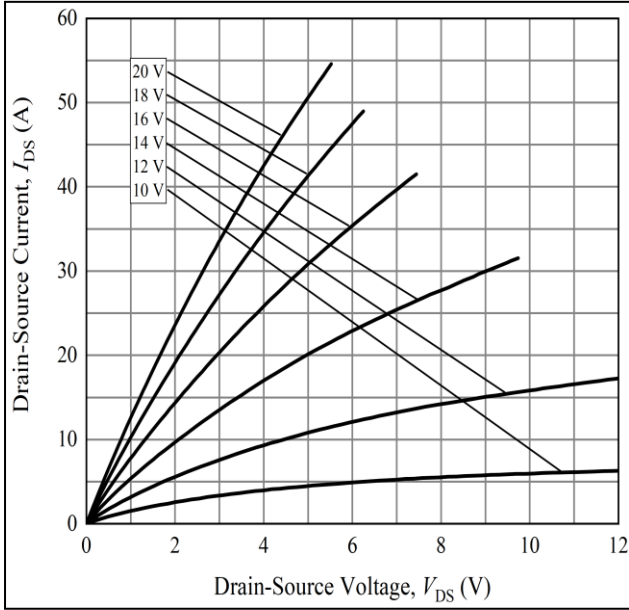


Figure 1: Typical Output Characteristics at $T_j=-55\text{ }^\circ\text{C}$

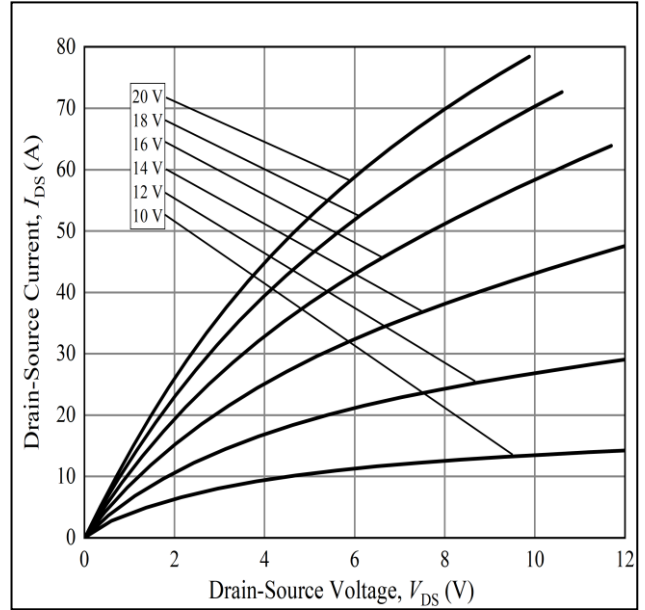


Figure 2: Typical Output Characteristics at $T_j=25\text{ }^\circ\text{C}$

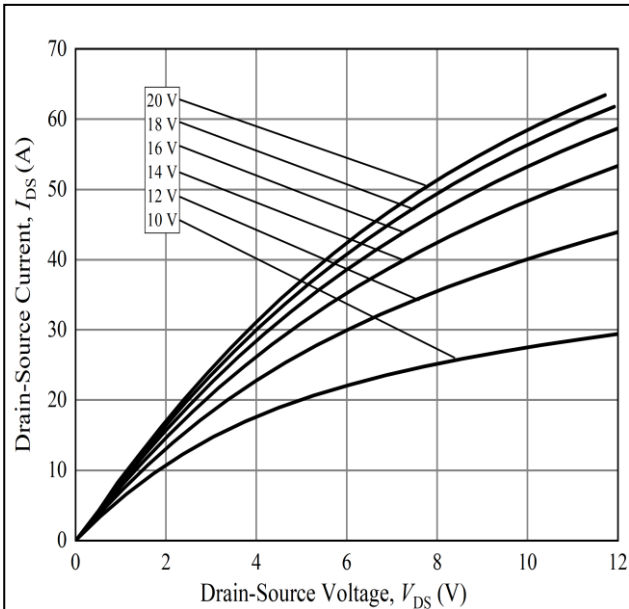


Figure 3: Typical Output Characteristics at $T_j=175\text{ }^\circ\text{C}$

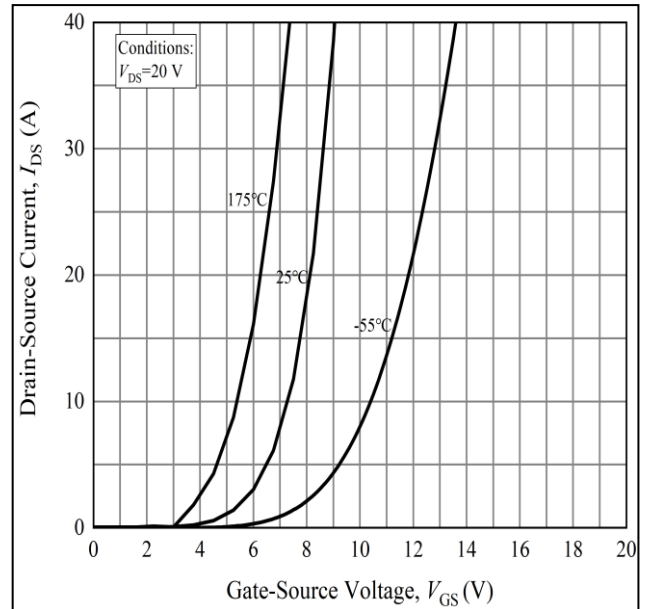


Figure 4: Typical Transfer Characteristics for Various Temperature

Typical Performance

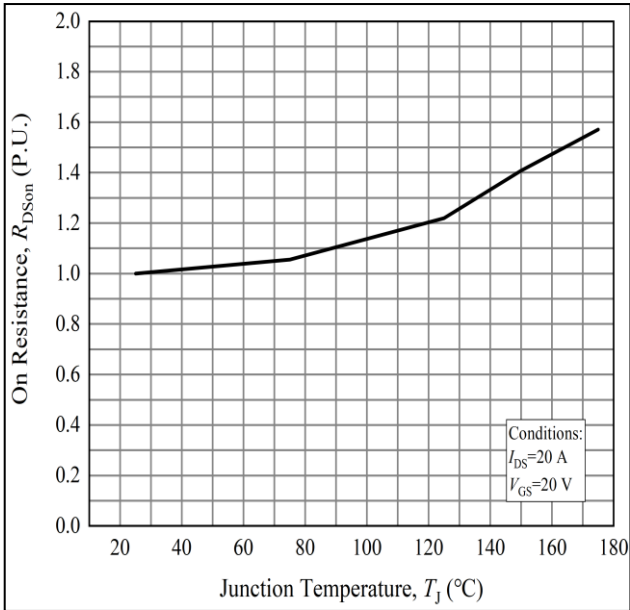


Figure 5: Normalized On-Resistance vs. Temperature

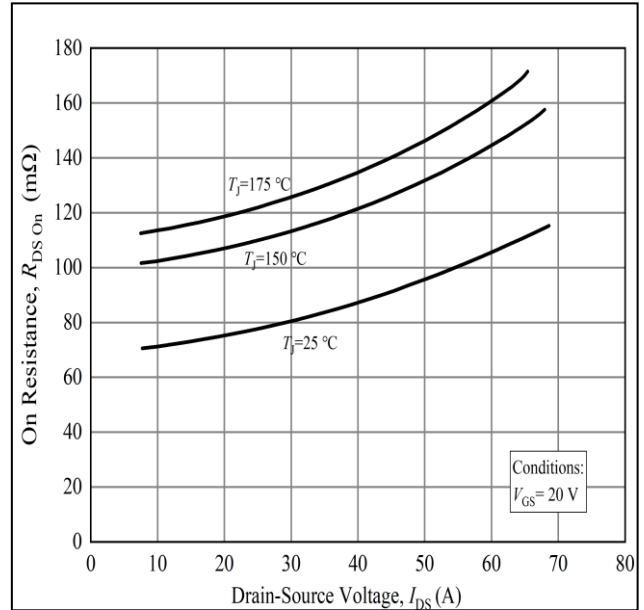


Figure 6: On-Resistance vs. Drain Current for Gate Various Temperatures

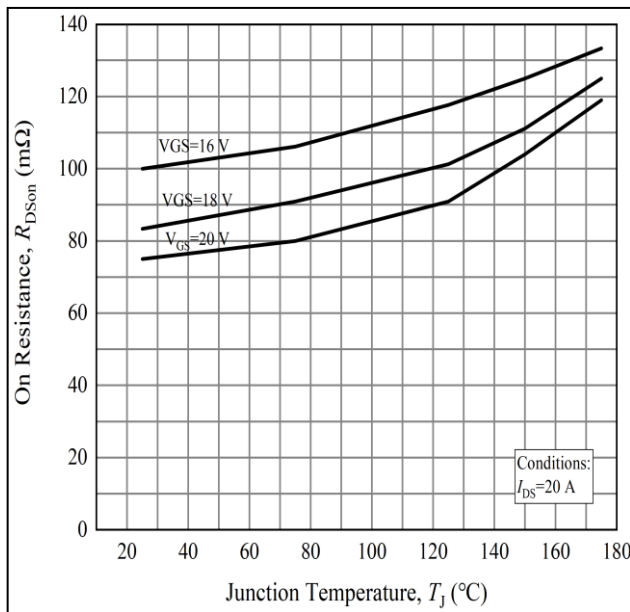


Figure 7: On-Resistance vs. Temperature for Various Voltage

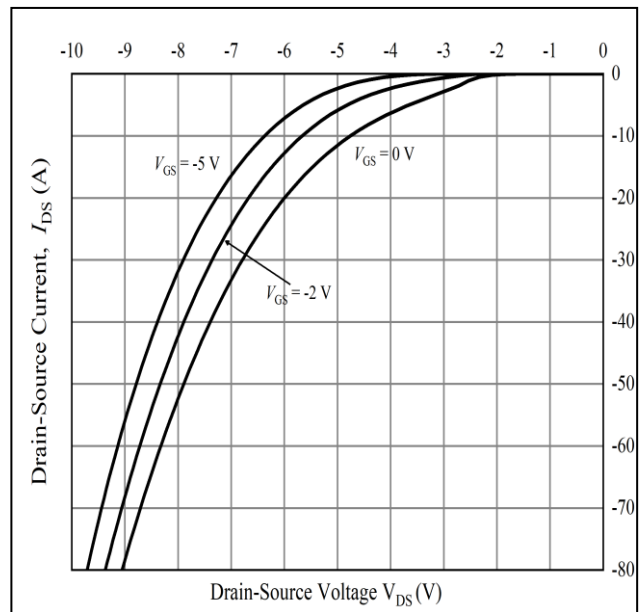


Figure 8: Typical Body Diode Characteristics at $T_J=-55\text{ }^\circ\text{C}$

Typical Performance

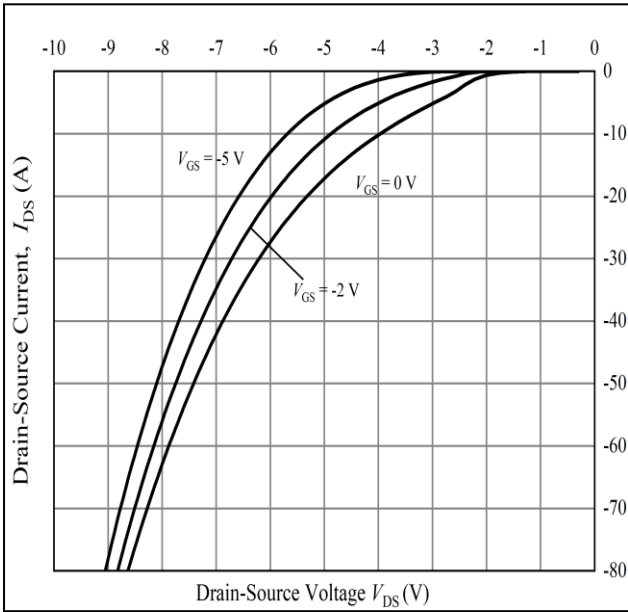


Figure 9: Typical Body Diode Characteristics at $T_j = 25\text{ }^\circ\text{C}$

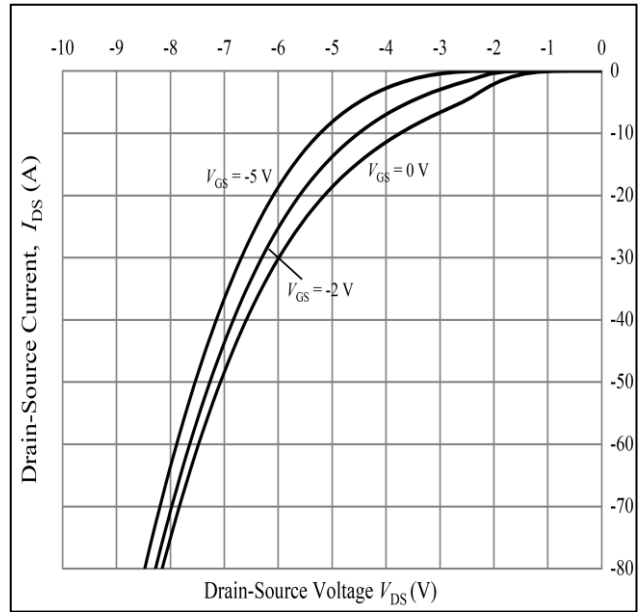


Figure 10: Typical Body Diode Characteristics at $T_j = 175\text{ }^\circ\text{C}$

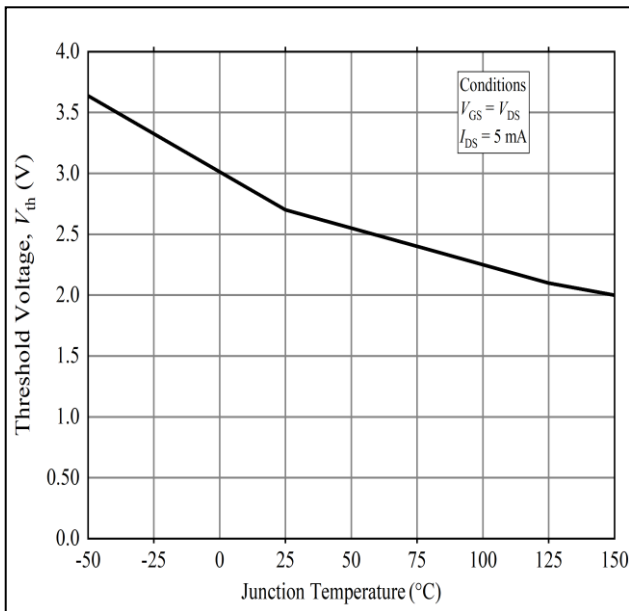


Figure 11: Typical Threshold Voltage vs. Temperature

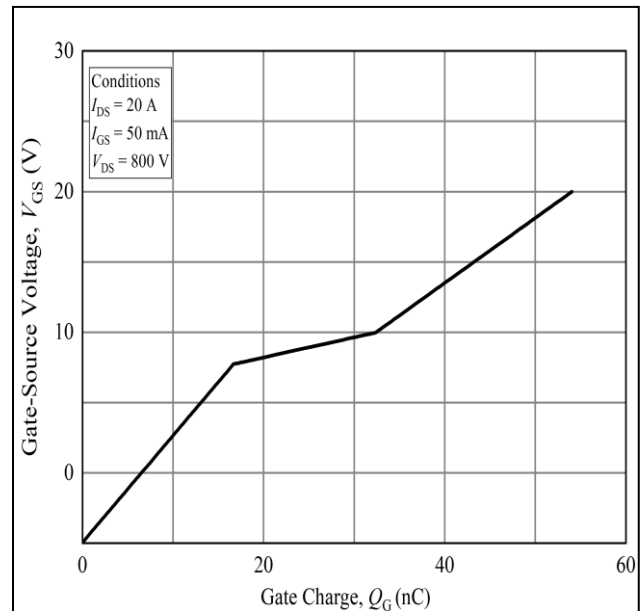


Figure 12: Typical Gate Charge Characteristics at $T_j = 25\text{ }^\circ\text{C}$

Typical Performance

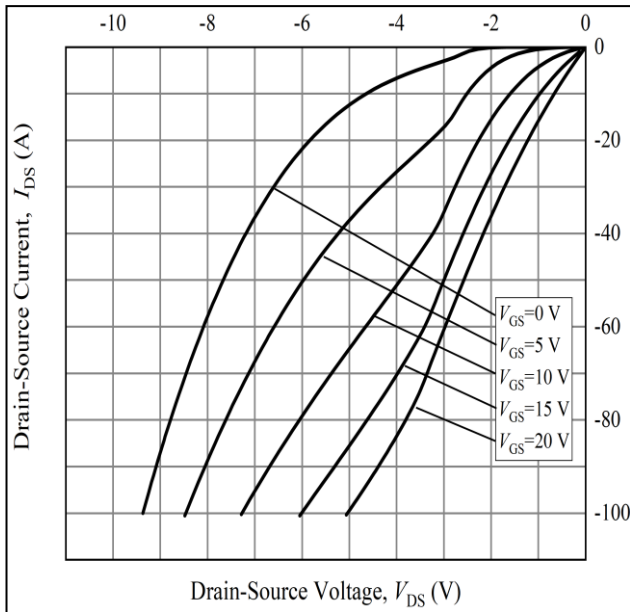


Figure 13: Typical 3rd Quadrant Characteristics
 $T_j = -55\text{ }^\circ\text{C}$

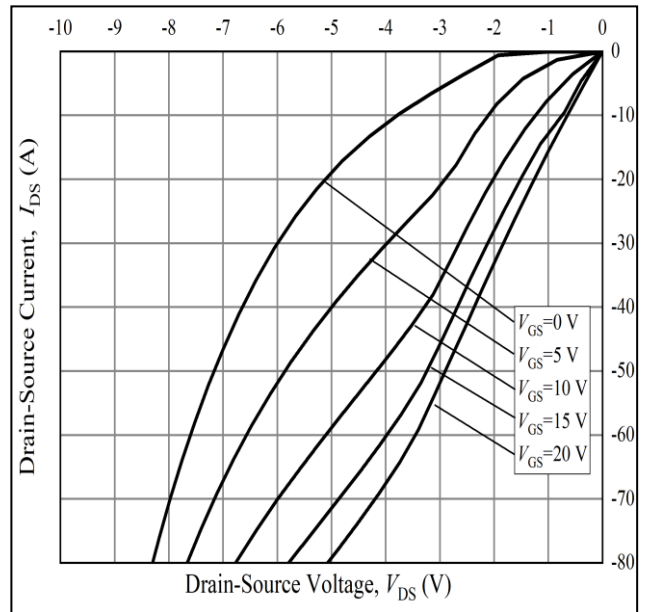


Figure 14: Typical 3rd Quadrant Characteristics at
 $T_j = 25\text{ }^\circ\text{C}$

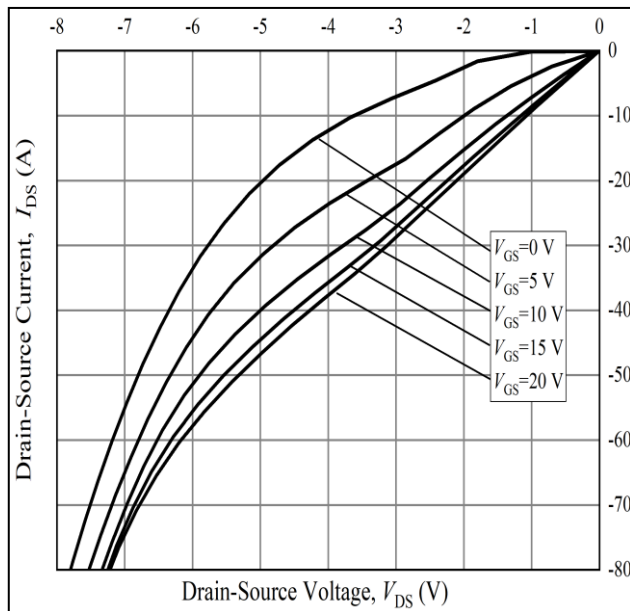


Figure 15: Typical 3rd Quadrant Characteristics
at $T_j = 175\text{ }^\circ\text{C}$

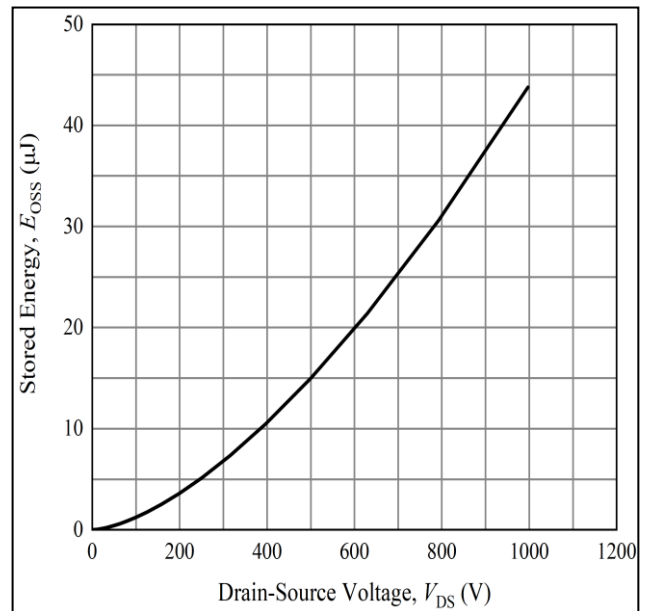


Figure 16: Typical Output Capacitor Stored Energy

Typical Performance

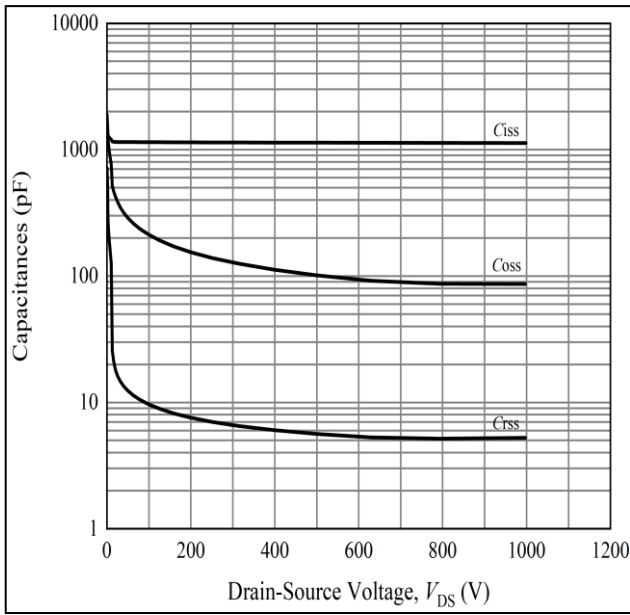


Figure 17: Typical Capacitances vs. Drain-Source Voltage

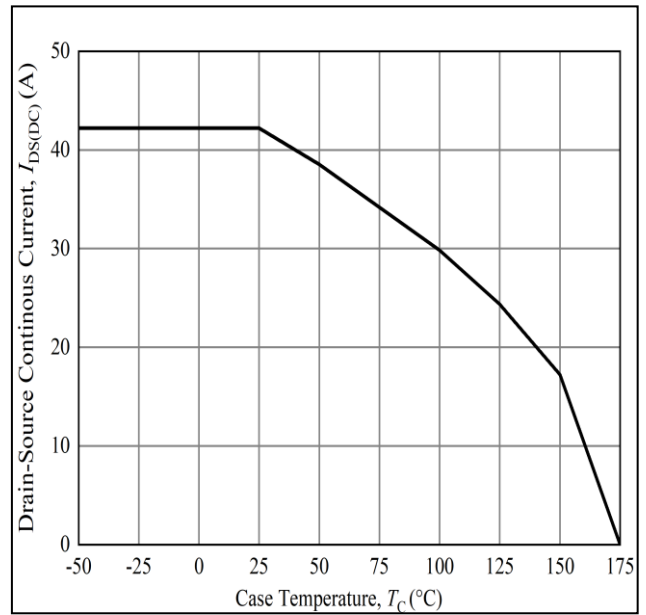


Figure 18: Continuous I_{DS} Current Derating Curve

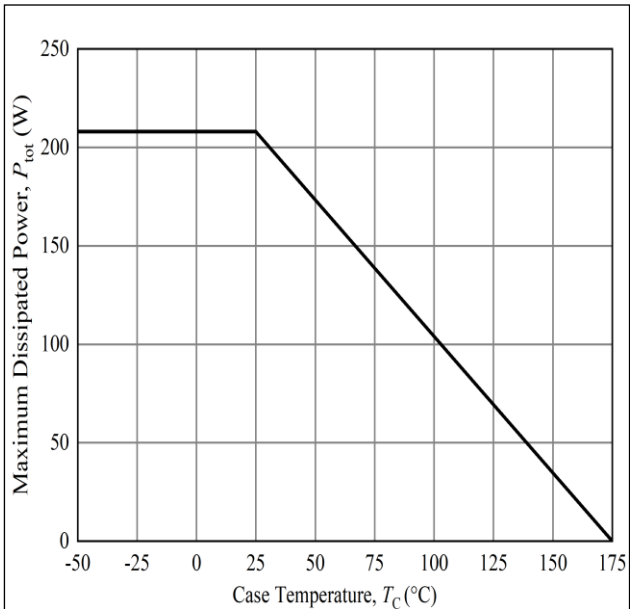


Figure 19: Power Dissipation Derating Curve

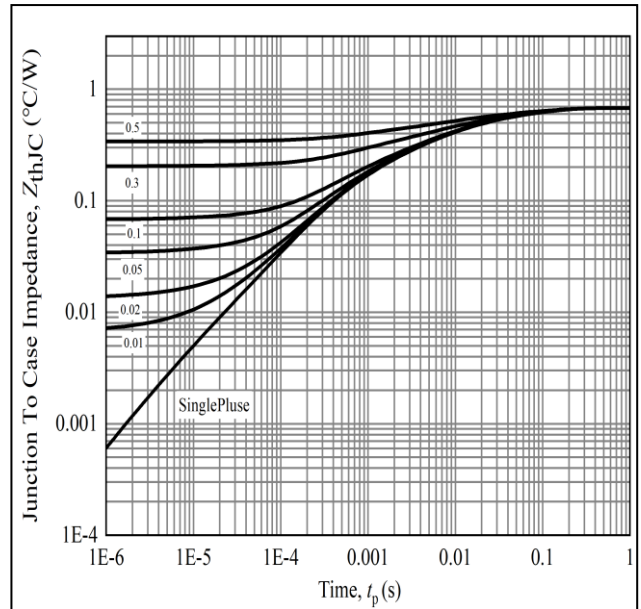


Figure 20: Typical Transient Thermal Impedance (Junction – Case) with Duty Cycle

Typical Performance

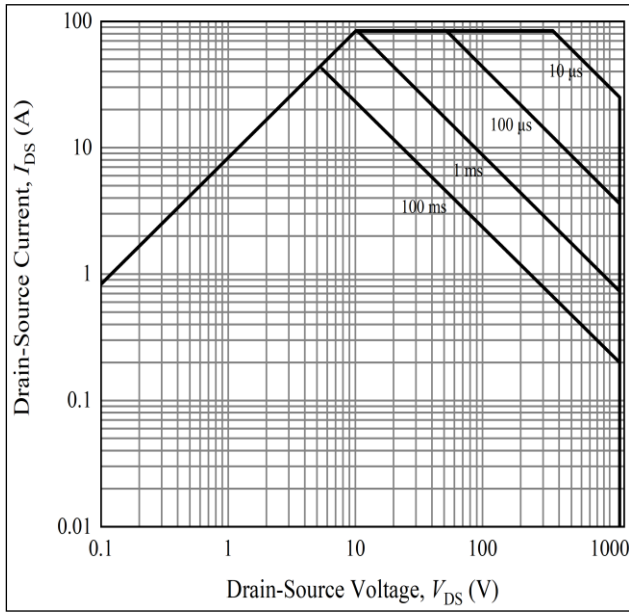


Figure 21: Safe Operate Area

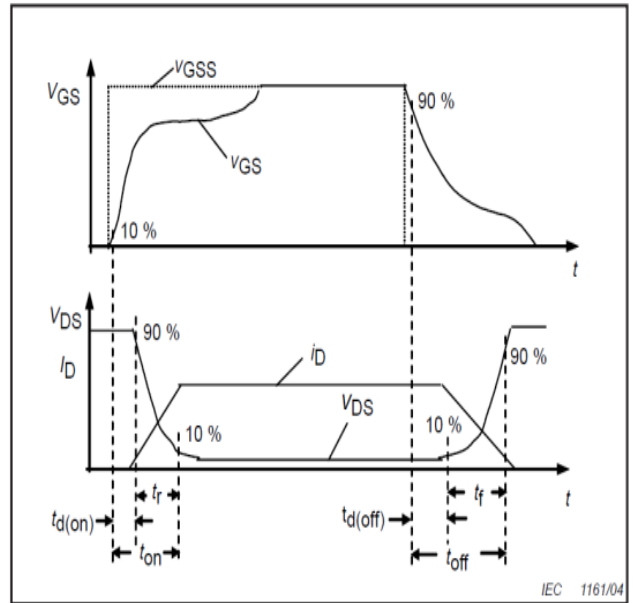


Figure 22: Resistive Switching Time Description

Test Circuit Schematic

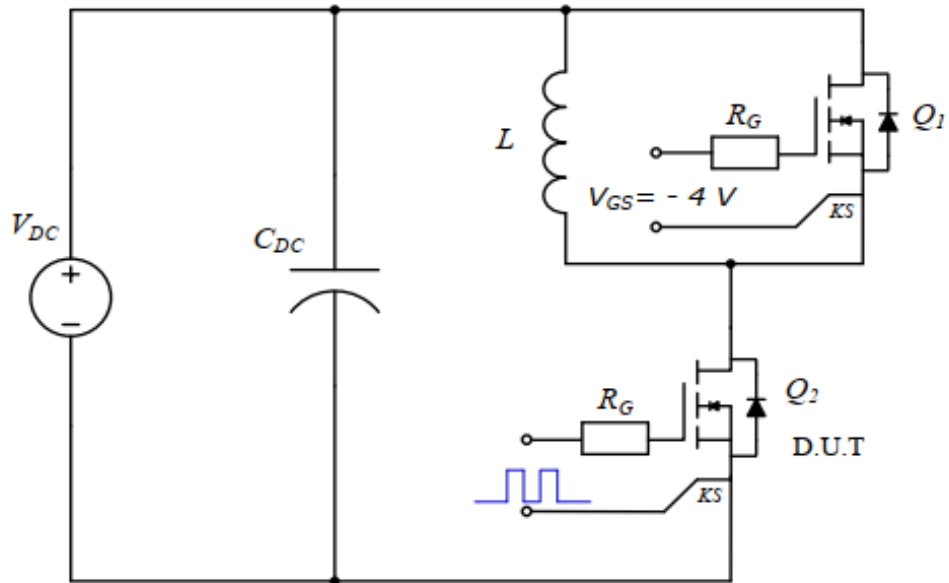
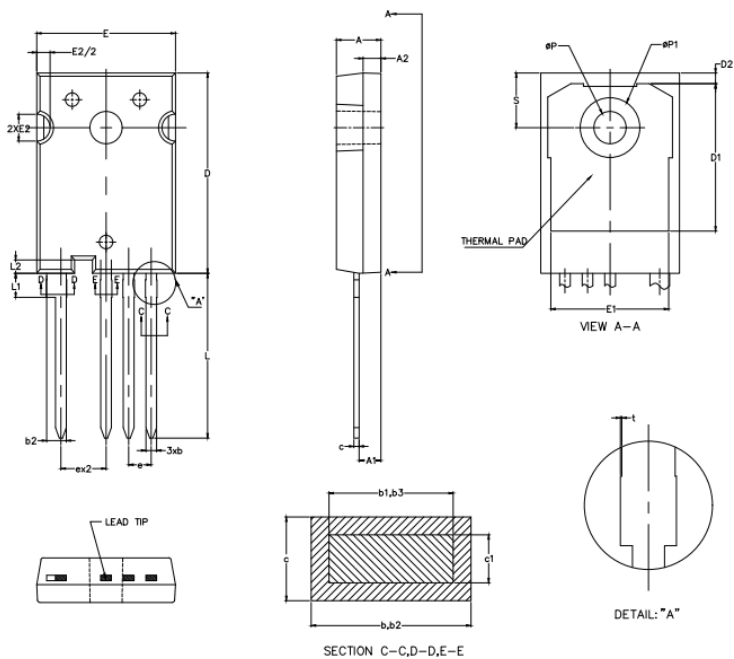


Figure 23: Clamped Inductive Switching Waveform Test Circuit

Package Dimensions

Package: TO-247-4



SYMBOLS	DIMENSIONS			
	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A	4.90	5.10	0.193	0.201
A1	2.31	2.51	0.091	0.099
A2	1.90	2.10	0.075	0.083
b	1.16	1.26	0.046	0.050
b1	1.15	1.22	0.045	0.048
b2	2.16	2.26	0.085	0.089
b3	2.15	2.22	0.085	0.087
c	0.59	0.66	0.023	0.026
c1	0.58	0.62	0.023	0.024
D	22.40	22.60	0.882	0.890
D1	16.25	16.85	0.640	0.663
D2	1.05	1.35	0.041	0.053
E	15.75	15.90	0.620	0.626
E1	13.26	—	0.552	—
E2	2.90	3.10	0.114	0.122
e	2.54BSC		0.1BSC	
L	18.30	18.60	0.720	0.732
L1	—	2.80	—	0.110
L2	—	1.50	—	0.059
ϕP	3.50	3.70	0.138	0.146
$\phi P1$	—	7.40	—	0.291
S	6.05	6.25	0.238	0.246
t	0.00	0.15	0.000	0.006

Revision History

Document Version	Description of Changes
Rev.1.0	Released

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安徽芯塔电子科技有限公司
TOPE Technologies Co., Ltd.
WuHu, Anhui, China 241002

Contact: sale@topelectronics.cn

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